

Appl. No. 10/706,380
Amdt. dated 09/23/2005
Response to Office Action of 06/02/2005

Attorney Docket No.: TS01-1674
N1085-90185

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A method for synthesizing a clock distribution circuit within an integrated circuit device, said device comprised of a plurality of functional circuits and placed on a substrate, said method comprising the steps of:

allocating at least one delaying circuit within each of said functional circuits;

fabricating an intra-functional clock distribution network within each of the functional circuits;

fabricating an inter-functional clock distribution network between each of the functional circuits;

determining a clock skew for the inter-functional clock distribution network; and

compensating for the clock of said inter-functional clock distribution network by inserting said delaying circuit at a terminal of said inter-function clock distribution network where wherein each of said functional circuits is connected to said inter-functional clock distribution network and said delaying circuit includes a plurality of delaying buffer circuits that are serially connected by a plurality of interconnecting wiring segments, each delaying buffer circuit having a first increment of delay and said interconnecting wiring segments having a second increment of delay.

2. (Original) The method of claim 1 wherein compensating for said clock skew of said inter-functional clock distribution network comprises the steps of:

determining a clock skew factor for one selected functional circuit connected to one selected terminal of said inter-functional clock distribution network; and

adjusting the delaying circuit within said one selected functional circuit to cancel out said clock skew factor.

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1 3. (Cancelled)

1 4. (Currently Amended) The method of claim [[3]] 1 wherein adjusting said
2 delaying circuit comprises the step of connecting a first quantity of said delaying buffer
3 circuits with a second quantity of said plurality of interconnecting wiring segments such
4 that a sum of the first increment of delay of said first quantity of the delaying buffer
5 circuits and the second quantity of delay of said interconnecting wiring segments is
6 equal to the clock skew factor.

1 5. (Currently Amended) An apparatus for synthesizing a clock distribution
2 circuit within an integrated circuit device, said device comprised of a plurality of
3 functional circuits and placed on a substrate, said apparatus comprising:

4 means for allocating at least one delaying circuit within each of said functional
5 circuits;

6 means for fabricating an intra-functional clock distribution network within each of
7 the functional circuits;

8 means for fabricating an inter-functional clock distribution network between each
9 of the functional circuits;

10 means for determining a clock skew for the inter-functional clock distribution
11 network; and

12 means for compensating for the clock of said inter-functional clock distribution
13 network by inserting said delaying circuit at a terminal of said inter-function clock
14 distribution network where wherein each of said functional circuits is connected to said
15 inter-functional clock distribution network and said delaying circuit includes a plurality of
16 delaying buffer circuits that are serially connected by a plurality of interconnecting wiring
17 segments, each delaying buffer circuit having a first increment of delay and said
18 interconnecting wiring segments having a second increment of delay.

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1 6. (Original) The apparatus of claim 5 wherein means for compensating for said
2 clock skew of said inter-functional clock distribution network comprises:

3 means for determining a clock skew factor for one selected functional circuit
4 connected to one selected terminal of said inter-functional clock distribution network;
5 and

6 means for adjusting the delaying circuit within said one selected functional circuit
7 to cancel out said clock skew factor.

1 7. (Cancelled)

1 8. (Currently Amended) The apparatus of claim ~~[[7]]~~ 5 wherein the means for
2 adjusting said delaying circuit comprises means for connecting a first quantity of said
3 delaying buffer circuits with a second quantity of said plurality of interconnecting wiring
4 segments such that a sum of the first increment of delay of said first quantity of the
5 delaying buffer circuits and the second quantity of delay of said interconnecting wiring
6 segments is equal to the clock skew factor.

1 9. (Currently Amended) An apparatus for synthesizing a clock distribution
2 circuit within an integrated circuit device, said device comprised of a plurality of
3 functional circuits and placed on a substrate, said apparatus comprising means for
4 executing the steps of:

5 allocating at least one delaying circuit within each of said functional circuits;

6 fabricating an intra-functional clock distribution network within each of the
7 functional circuits;

8 fabricating an inter-functional clock distribution network between each of the
9 functional circuits;

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10 determining a clock skew for the inter-functional clock distribution network; and
11 compensating for the clock of said inter-functional clock distribution network by
12 inserting said delaying circuit at a terminal of said inter-function clock distribution
13 network where wherein each of said functional circuits is connected to said inter-
14 functional clock distribution network and said delaying circuit includes a plurality of
15 delaying buffer circuits that are serially connected by a plurality of interconnecting wiring
16 segments, each delaying buffer circuit having a first increment of delay and said
17 interconnecting wiring segments having a second increment of delay.

1 10. (Original) The apparatus of claim 9 wherein compensating for said clock skew
2 of said inter-functional clock distribution network comprises the steps of:

3 determining a clock skew factor for one selected functional circuit connected to
4 one selected terminal of said inter-functional clock distribution network; and

5 adjusting the delaying circuit within said one selected functional circuit to cancel
6 out said clock skew factor.

1 11. (Cancelled)

1 12. (Currently Amended) The apparatus of claim ~~[[11]]~~ 9 wherein adjusting said
2 delaying circuit comprises the step of connecting a first quantity of said delaying buffer
3 circuits with a second quantity of said plurality of interconnecting wiring segments such
4 that a sum of the first increment of delay of said first quantity of the delaying buffer
5 circuits and the second quantity of delay of said interconnecting wiring segments is
6 equal to the clock skew factor.

1 13. (Currently Amended) A clock distribution circuit within an integrated circuit
2 device, said device comprised of a plurality of functional circuits and placed on a
3 substrate, said clock distribution circuit comprising:

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4 at least one delaying circuit placed within each of said functional circuits;
5 an intra-functional clock distribution network within each of the functional circuits;
6 and
7 an inter-functional clock distribution network between each of the functional
8 circuits;
9 wherein a clock skew for the inter-functional clock distribution network is
10 compensated by inserting said delaying circuit at a terminal of said inter-function clock
11 distribution network ~~where~~ wherein each of said functional circuits is connected to said
12 inter-functional clock distribution network and said delaying circuit includes a plurality of
13 delaying buffer circuits that are serially connected by a plurality of interconnecting wiring
14 segments, each delaying buffer circuit having a first increment of delay and said
15 interconnecting wiring segments having a second increment of delay.

1 14. (Original) The clock distribution circuit of claim 12 wherein compensating for
2 said clock skew of said inter-functional clock distribution network comprises the steps
3 of:

4 determining a clock skew factor for one selected functional circuit connected to
5 one selected terminal of said inter-functional clock distribution network; and

6 adjusting the delaying circuit within said one selected functional circuit to cancel
7 out said clock skew factor.

1 15. (Cancelled)

1 16. (Currently Amended) The clock distribution circuit of claim ~~[[15]]~~ 13 wherein
2 adjusting said delaying circuit comprises the step of connecting a first quantity of said
3 delaying buffer circuits with a second quantity of said plurality of interconnecting wiring
4 segments such that a sum of the first increment of delay of said first quantity of the

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5 delaying buffer circuits and the second quantity of delay of said interconnecting wiring
6 segments is equal to the clock skew factor.

1 17. (Currently Amended) A integrated circuit synthesizing apparatus for
2 synthesizing an integrated circuit device, said device comprised of a plurality of
3 functional circuits and placed on a substrate, said integrated circuit synthesizing
4 apparatus executing the steps of:

5 synthesizing a clock distribution circuit within said integrated circuit device, said
6 synthesizing comprising the steps of:

7 allocating at least one delaying circuit within each of said functional circuits;

8 fabricating an intra-functional clock distribution network within each of the
9 functional circuits;

10 fabricating an inter-functional clock distribution network between each of the
11 functional circuits;

12 determining a clock skew for the inter-functional clock distribution network; and

13 compensating for the clock of said inter-functional clock distribution network by
14 inserting said delaying circuit at a terminal of said inter-function clock distribution
15 network ~~where~~ wherein each of said functional circuits is connected to said inter-
16 functional clock distribution network and said delaying circuit includes a plurality of
17 delaying buffer circuits that are serially connected by a plurality of interconnecting wiring
18 segments, each delaying buffer circuit having a first increment of delay and said
19 interconnecting wiring segments having a second increment of delay.

1 18. (Original) The integrated circuit synthesizing apparatus of claim 17 wherein
2 compensating for said clock skew of said inter-functional clock distribution network
3 comprises the steps of:

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4 determining a clock skew factor for one selected functional circuit connected to
5 one selected terminal of said inter-functional clock distribution network; and

6 adjusting the delaying circuit within said one selected functional circuit to cancel
7 out said clock skew factor.

1 19. (Cancelled)

1 20. (Currently Amended) The integrated circuit synthesizing apparatus of claim
2 [[19]] 17 wherein adjusting said delaying circuit comprises the step of connecting a first
3 quantity of said delaying buffer circuits with a second quantity of said plurality of
4 interconnecting wiring segments such that a sum of the first increment of delay of said
5 first quantity of the delaying buffer circuits and the second quantity of delay of said
6 interconnecting wiring segments is equal to the clock skew factor.

1 21. (Currently Amended) A medium for retaining a computer program which,
2 when executed on a computing system, executes a process for synthesizing a clock
3 distribution circuit within an integrated circuit device, said device comprised of a plurality
4 of functional circuits and placed on a substrate, said process comprising the steps of:

5 allocating at least one delaying circuit within each of said functional circuits;

6 fabricating an intra-functional clock distribution network within each of the
7 functional circuits;

8 fabricating an inter-functional clock distribution network between each of the
9 functional circuits;

10 determining a clock skew for the inter-functional clock distribution network; and

11 compensating for the clock of said inter-functional clock distribution network by
12 inserting said delaying circuit at a terminal of said inter-function clock distribution

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13 network where wherein each of said functional circuits is connected to said inter-
14 functional clock distribution network and said delaying circuit includes a plurality of
15 delaying buffer circuits that are serially connected by a plurality of interconnecting wiring
16 segments, each delaying buffer circuit having a first increment of delay and said
17 interconnecting wiring segments having a second increment of delay.

1 22. (Original) The medium of claim 20 wherein compensating for said clock skew
2 of said inter-functional clock distribution network comprises the steps of:

3 determining a clock skew factor for one selected functional circuit connected to
4 one selected terminal of said inter-functional clock distribution network; and

5 adjusting the delaying circuit within said one selected functional circuit to cancel
6 out said clock skew factor.

1 23. (Cancelled)

1 24. (Currently Amended) The medium of claim ~~[[23]]~~ 21 wherein adjusting said
2 delaying circuit comprises the step of connecting a first quantity of said delaying buffer
3 circuits with a second quantity of said plurality of interconnecting wiring segments such
4 that a sum of the first increment of delay of said first quantity of the delaying buffer
5 circuits and the second quantity of delay of said interconnecting wiring segments is
6 equal to the clock skew factor.